ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 2.114

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

A NOVEL TOPOLOGY FOR MULTILEVEL INVERTER USING FPGA

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ABSTRACT

Multi level inverter has been dominating the engineering field over the last few decades. However the output waveform of the present inverter possesses undesirably large harmonic content. The main purpose of this paper is to implement a multilevel inverter with output waveform having less total harmonic distortion. The novel topology introducedhere is known as the reverse voltage topology. The notable advantage of this topology is the minimum requirement of components and carriers signals. The end result is a substantial reduction in the overall cost and complexity. Other advantages include lower Total Harmonic Distortion (THD), less stress on the power switches and higher efficiency. FPGA plays the role of the controller. Finally, a prototype of the nine-level proposed topology is built and tested to show the performance of the inverter by experimental results. The proposed topology and its control method are explained and detailed simulation has been carried out in MATLAB/ simulink.

Keywords: Multilevel inverter, power electronics, Phase Disposition SPWM, Reverse voltage topology, FPGA.

INTRODUCTION

In the simplest of terms an inverter performs dc to ac conversion. A typical two level inverter faces many problems such as high switching frequency, less efficiency, high cost and high switching losses. The concept of multilevel converters evolved during the 1970s.Conventional inverters have been pushed aside by multilevel inverters due to their various advantages. The compatible structure of multilevel inverters makes it possible to reach high voltages with lesser harmonic content and lower electromagnetic interference. Various PWM strategies are required to get high quality output which leads to high switching losses. Higher number of semiconductor switches is required to perform the power conversion in small voltage step. Multilevel inverter produces a staircase output waveform with lesser total harmonic distortion and more resemblance to a sinusoidal waveform. The advantages of multilevel inverter are improvement in staircase waveform quality, less input current distortion and lower electromagnetic interference. Multilevel inverters are used in drives, PV systems, and automotive applications. The harmonic content of the output voltage waveform decreases as the number of output voltage increases. Many topologies have been introduced for multilevel inverters..A new multilevel inverter with reduced number of components is presented here.

This inverter is more efficient since it has a component which operates the switching power devices at line frequency, which leads to simpler and reliable control. This project is based on nine-level inverter with reverse voltage topology which requires less number of switches than conventional topologies. Here the generation of carrier based PWM scheme is using phase deposition method and we can control output voltage and frequency and reduce the harmonic components in load currents. In phase deposition SPWM we use ((n-1)/2) carriers to drive the inverter and all carrier waveforms are in phase. The simulation results and experimental results are presented

REVERSE VOLTAGE TOPOLOGY

Conventional cascaded multilevel inverters require large number of switches and the power switches are combined to generate an output in positive and negative polarities. In the proposed multilevel inverter there is no need to use all the switches in high frequency. This topology separates the output voltage into level and polarity generation parts. Level generation part generates levels in positive polarity and the polarity generation part generates the polarity of the output voltage. Level generation part needs high frequency switches and polarity generation part requires low-frequency switches operating at line frequency.

Figure 1 shows the general block diagram of reverse voltage topology. This multilevel inverter can be used to produce higher voltage levels by increasing the middle section of Fig 2.Ninelevel inverter with reverse voltage topology requires less switches and it can be applied to three phase application. The Phase

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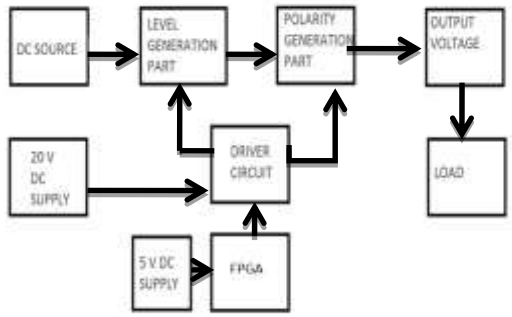
Disposition (PD) SPWM needs only half the number of conventional carriers for SPWM.PD-SPWM for nine-level conventional converters requires eight carriers, but in the proposed system only four carriers are needed. To generate polarity, the positive voltage is fed to the polarity generation part. Multilevel inverter control with less number of carriers is the main advantage. Separate DC source are needed for this topology. The proposed multilevel inverter has betterefficiency than conventional multilevel inverter.

Figure: 1



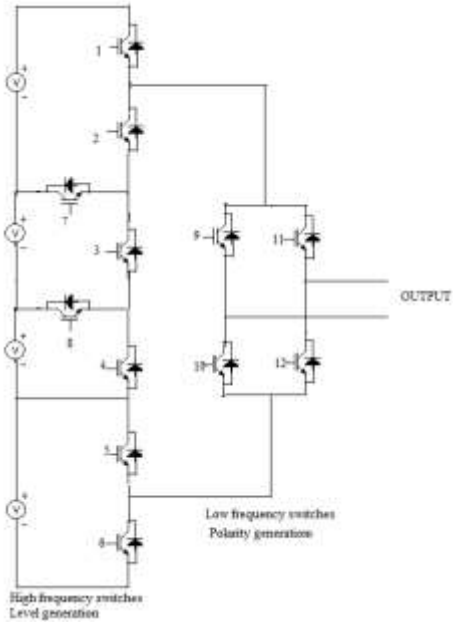
Block Diagram

The left portion of the circuit in Fig.2 generates the required output levels and the right portion of the circuit generates the polarity of the output voltage. The right portion of the circuit is called polarity generation part; it reverses the output of the level generation part when the voltage polarity requires to be changed for negative polarity.

Modes Of Operation

The switching modes are selected such that the switching transitions become minimal for avoiding the unwanted voltage levels. This will minimize switching power dissipation. The sequence of switches (2-3-4-5), (2-3-4-6), (2-3-8-6), (2-7-6) and (1-6) are used for levels 0 up to 4, respectively. The output voltage is the sum of voltage sources. Table I shows the switching sequences

Figure: 2



Nine level inverter with reverse voltage topology.

CONTROL CIRCUITRY

FPGA(Field Programmable Gate Array) is used as the controller. It is an array (matrix) of logic gates that can be arranged to perform any possible (combinational and/or sequential) logic function.They can be programmed to perform any functions and they can be programmed “in the field”,i.e., the device as it comes out of the production line is not committed to any specific functionality. The FPGA configuration is generally specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC).Contemporary FPGAs have large resources of logic gates and RAM blocks to implement complex digital computations. As FPGA designs employ very fast I/Os and bidirectional data buses it becomes a challenge to verify correct timing of valid data within setup time and hold time. Floor planning enables resources allocation within FPGA to meet these time constraints. FPGAs can be used to implement any logical function that an ASIC could perform. The ability to update the functionality after shipping, partial re-configuration of a portion of the design and the low non-recurring engineering costs relative to an ASIC design (not withstanding the generally higher unit cost), offer advantages for many applications.FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together" – somewhat like many (changeable) logic gates that can be inter-wired in different configurations. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like ANDandXOR. In most FPGAs, the logic blocks also

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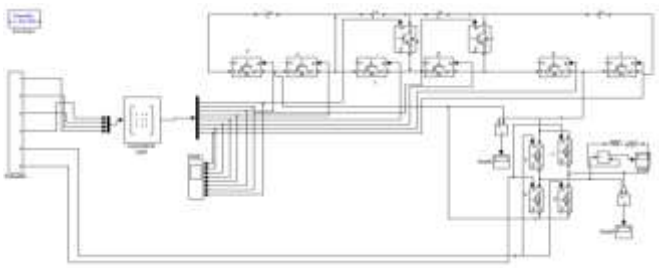
include memory elements, which may be simple flip-flops or more complete blocks of memory.
Some FPGAs have analog features in addition to digital functions. The most common analog feature is programmable slew rate and drive strength on each output pin, allowing the engineer to set slow rates on lightly loaded pins that would otherwise ring or couple unacceptably, and to set stronger, faster rates on heavily loaded pins on high-speed channels that would otherwise run too slowly. Another relatively common analog feature is differential comparators on input pins designed to be connected to differential signaling channels. A few "mixed signal FPGAs" have integrated peripheral analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) with analog signal conditioning blocks allowing them to operate as a system-on-a-chip. Such devices blur the line between an FPGA, which carries digital ones and zeros on its internal programmable interconnect fabric, and field-programmable analog array (FPAA), which carries analog values on its internal programmable interconnect fabric.

RESULTS AND DISCUSSION

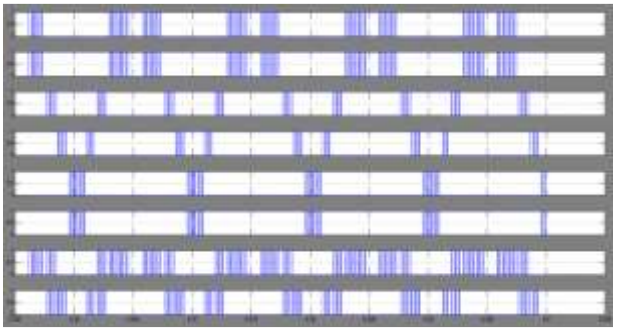
Modulation techniques are used in multilevel inverter to synthesis a controlled output voltage. There are various modulation techniques, of which phase disposition pulse width modulation is used here. Simulation of the proposed topology of multilevel inverter is performed using mat lab.Simulation results are given below. Here phase disposition SPWM is used for driving the high frequency switches and low frequency polarity generation part drive signals are generated with the line frequency (50Hz), and they only change at zero-voltage crossings. In this proposed topology, a-phase modulation signal is compared with (n-1)/2 carriers for an n level inverter and all the carriers are in phase. Since this converter works only in positive polarity, this topology requires half of the conventional carriers for SPWM controller. DC power supplies are adjusted to 50V and the switching frequency is 4KHz.Output voltage is 400VP-P. The simulation diagram of proposed multilevel inverter with inductive load is shown in Figure6.The subsystem in Fig shows the phase disposition PWM generation.

Figure: 3



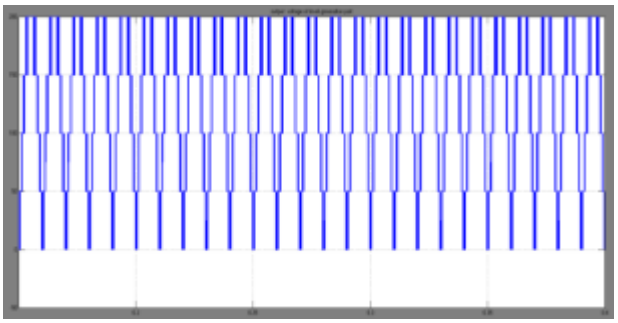
Simulation Diagram

Figure: 4



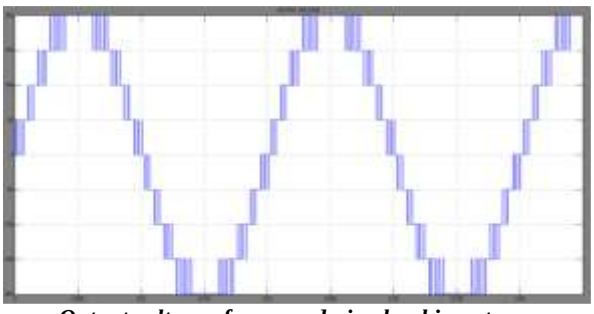
Complete gate signal for level generation part

Figure: 5



Voltage of the level genearation part

Figure: 6



Output voltage of proposed nine level inverter.

Figure: 7

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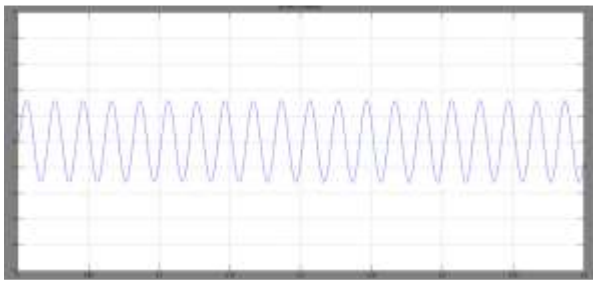

Output current of proposed nine level inverter.

CONCLUSION

In the proposed topology ,switching operations are separated into high and low frequency parts. It has many advantages such asit reduces the complexity in control method, low cost and has less Total Harmonic Distortion. Hence proposed topology is more convenient than conventional cascaded inverter topology. The background study based on the various aspects of the PWM firing scheme was analyzed. The carrier based PWM scheme using the Phase Disposition (PD) strategy is used here.Theinverter finds its peculiar applications in HVDC, FACTS,EV,PV,UPS and industrial drives.

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